8.3.1 A SINGLE-BOARD PREPROCESSOR AND PULSE GENERATOR

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The Aeronomy Laboratory of NOAA has designed and built a single-board, programmable radar controller for use with VHF ST radars. The controller consists of a coherent integrator preprocessor and a radar pulse generator, both described here, as well as interfaces to an antenna beam switch and a receiver bandwidth switch. The controller occupies a single slot in a Data General Nova or Eclipse computer. The integrator and pulse generator take advantage of high density, dual-port FIFO chips such as the 512 x 9 MOSTEK MK 4501. These FIFOs have separate input and output ports and independent read and write cycles with cycle times of less than 200 ns, making them very fast and easy to interface.

A simple block diagram of the coherent integrator is shown in Figure 1. At the completion of each ADC conversion, the 8-bit data from each receiver channel is latched into a register. The two channels are alternately placed at one input of the 16-bit adder. During the first interpulse period (IPP) the other input to the adder is set to zero and the data word is written directly into the FIFO. During successive IPPs, the data words are read from the FIFO, added to the incoming data from the corresponding range gate and rewritten to the FIFO. After the desired number of coherent additions have been completed, the data read from the FIFO is sent to the computer via the DMA channel, while the incoming data are being added to zero, beginning the cycle again. When a specified number of coherently averaged points for each range gate have been sent to the computer, the device is done and can interrupt the computer program. A status register, read from software, indicates errors such as adder overflow, FIFO overflow, and missed data points.

The integrator is designed to handle inputs from one receiver (2 channels) with 1 sec sample spacing. The timing could probably be adjusted for 500 ns samples, and additional receivers could be processed without any hardware modification by using one integrator board for each receiver. The design could also be altered to multiplex more channels onto a single board, but the maximum sampling rate would consequently be reduced.

The pulse generator is based on controllers designed by R. F. Woodman for the Arecibo and SOUSY radars using a "recirculating memory" scheme. Figure 2 shows the basic circuitry of the Aeronomy Laboratory device. The output lines of the pulse generator are the TR switch control pulse, the transmitter (Tx) logic pulse, and the sample gates. The state of each line changes according to the state of a specified bit of the FIFO memory as the data words are sequentially latched into an output register. The remaining bits of the FIFO word represent the number of 1-μsec clock cycles for that particular state to be held on the output latch. When that number is counted down to zero, a READ pulse is created and the next FIFO word is read into the output latch and the counter. The last word in the sequence is indicated by setting one bit (LAST) which creates a retransmit (RETRANS) signal. The retransmit function of the FIFO nondestructively resets the internal read pointer so that the data may be reread from the beginning.

The FIFO is loaded with the proper pulse sequence by a software DATA OUT (DOB) command and may be read back by a DATA IN (DIB) instruction. Once a START command is executed, the pulse generator will run continuously without further computer intervention. It can be stopped without destroying the FIFO

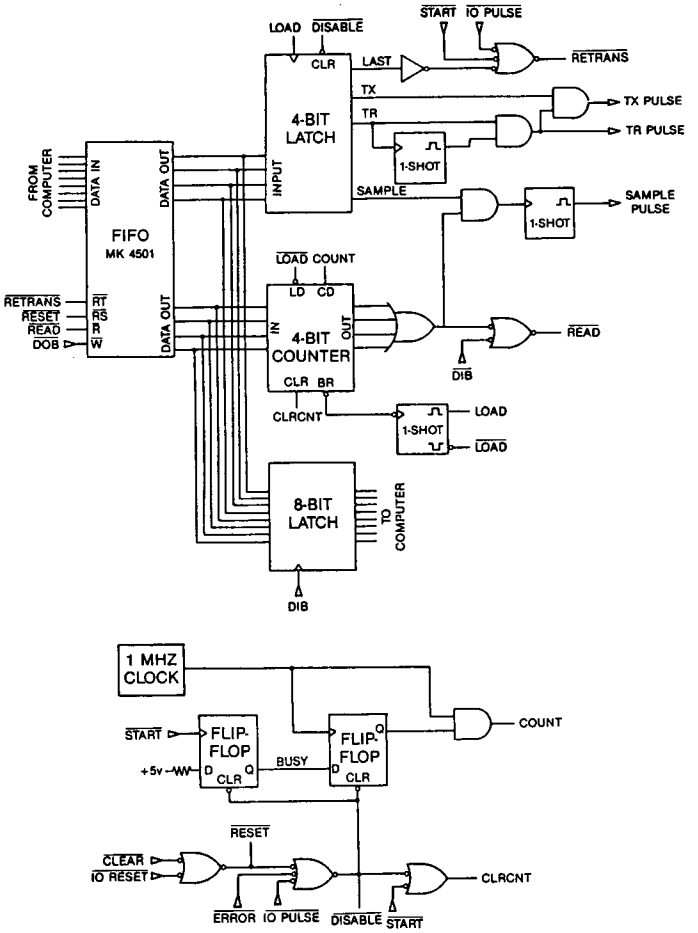

Figure 1. Coherent integrator block diagram.

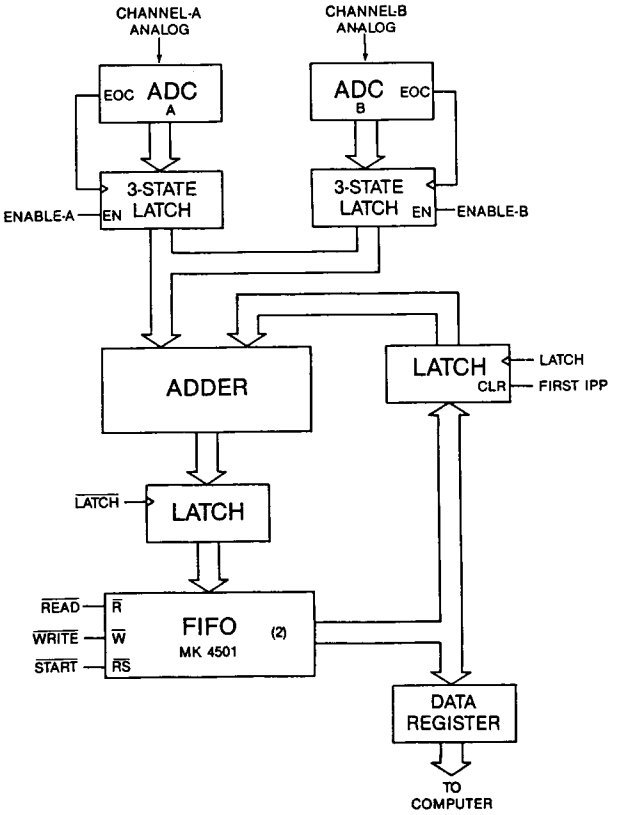

Figure 2. Radar pulse generator.

contents by a software IOPULSE command. A software CLEAR or hardware IORESET will reset the internal read and write pointers for rewriting the FIFO contents.

A number of safety features are built into the hardware. The TR pulse is gated with a fixed-length pulse to prevent the TR from accidently being turned on too long. The Tx pulse is allowed on only while the TR pulse is on. Any command that halts the pulse generator also clears the output lines. The ninth bit of the FIFO is used for parity. If a parity error is detected after a FIFO read cycle, the pulse generator is stopped and the computer program is interrupted.

In the pulse generator actually built, two FIFOs are used in parallel so that 8 lines are available for pulse signals and 8 lines for counting. Two of the additional signal lines are set up for Tx pulse coding. Coherent integration of the coded returns can be done in the preprocessor part of the board, but the decoding must be done in software.

The Aeronomy Laboratory has built three of these preprocessor/pulse generator devices. They each occupy about half of an MDB Systems I/O board, the other half being used by the vendor-supplied interfacing to the Data General I/O bus. One such board was used during the 1985 PRE-STORM program and others will be installed in Pacific Ocean ST radars on Ponape and Christmas Island. Compared to previous systems that used software coherent integration and manually controlled pulse generator boxes, this design offers great advantages in speed, flexibility, and radar efficiency.